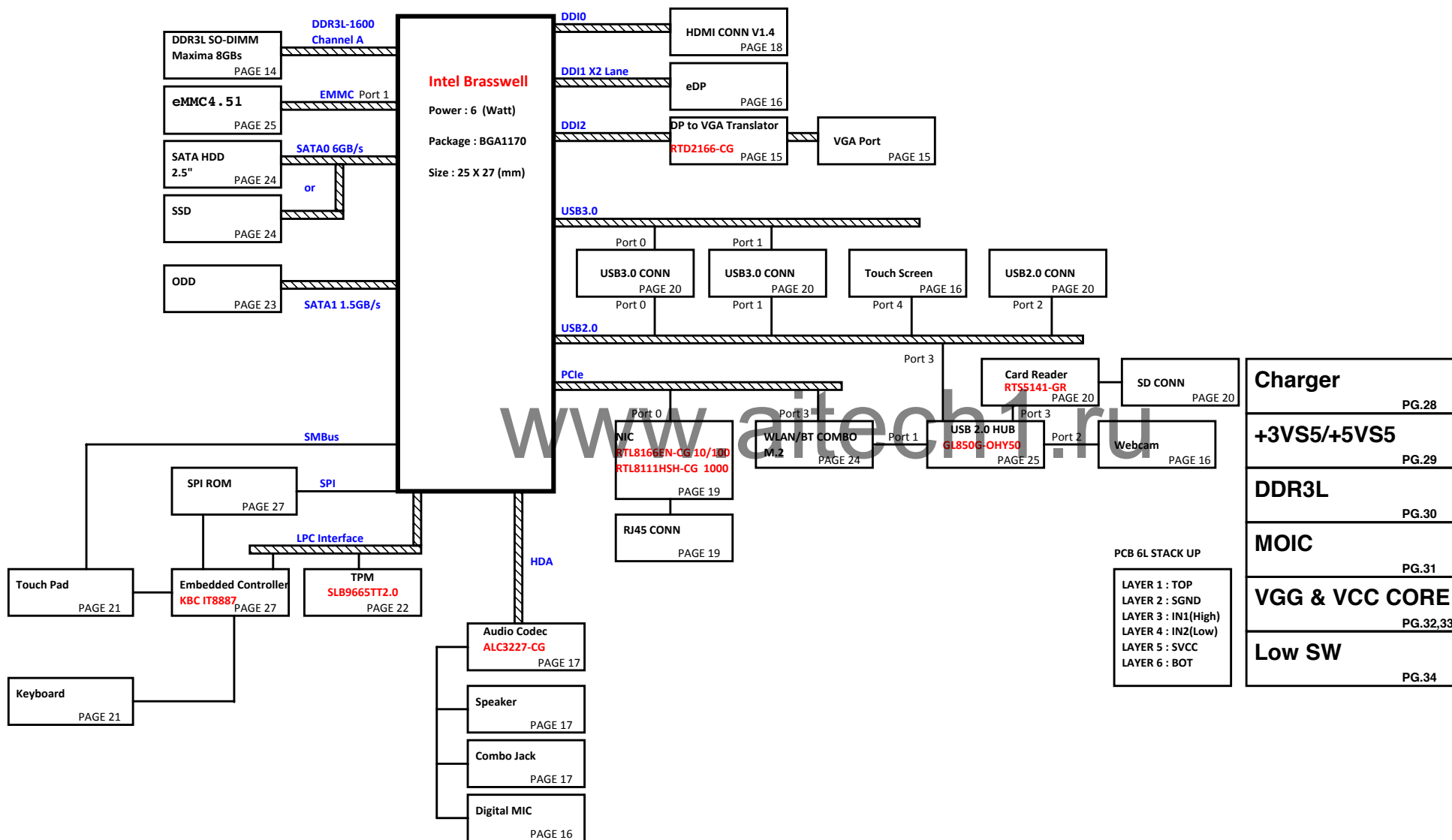


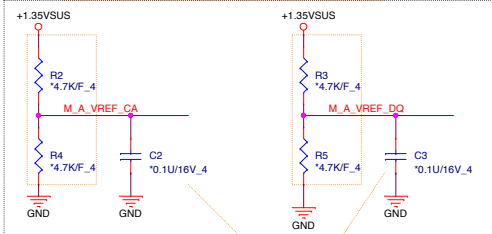
# NFL-C BSW 14"

## Intel Braswell-M Platform Block Diagram



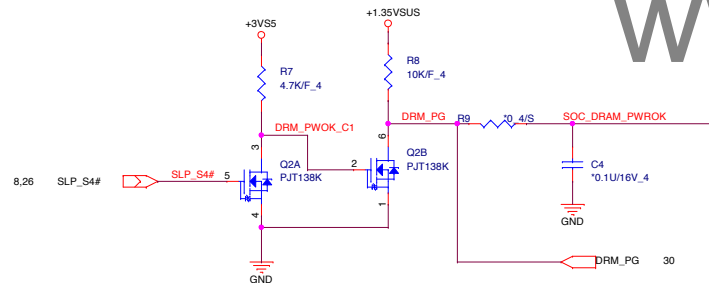
ROUTE ALL VREF POWER SIGNALS AS THICK TRACES

PLACE TWO 4.7K RESISTORS CLOSE TO CPU PINS ON M\_VREF  
ROUTE THE VREF POWER SIGNALS WITH THICK TRACES

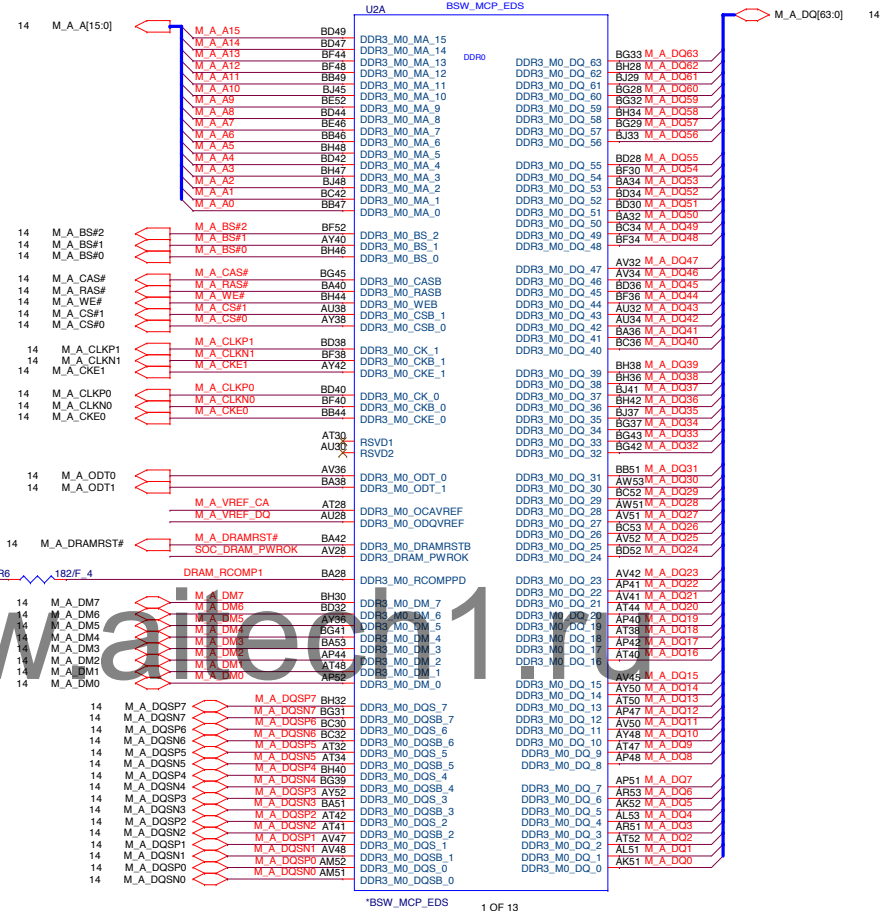


PLACE 0.1uF CAP CLOSE TO CPU

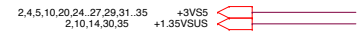
02/09 No Stuff Vref circuitry from SOC pages.  
VOLTAGE DIVIDER FOR VREF IS FOR DDR3L DIMMS ONLY. SOC DOES NOT DRIVE VREF.  
Follow to BRASWELL SOC EDS AND PDG FOR MORE DETAILS ABOUT DDR VREF



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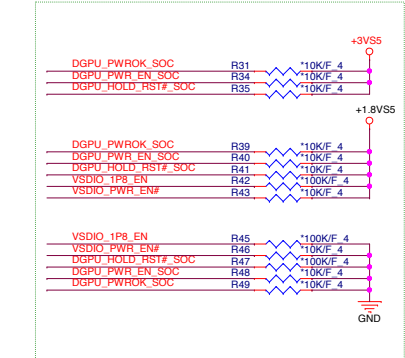
3,5,10,20,24,27,29,31,35 +3VS5  
3,10,14,30,35 +1.35VSUS



	U2B	BSW_MCP_EDS
BD5	DDR3, M1, MA_15	DOR1_A
BD6	DDR3, M1, MA_14	
BF6	DDR3, M1, MA_13	
B85	DDR3, M1, MA_12	
B94	DDR3, M1, MA_11	
BE2	DDR3, M1, MA_10	
BD10	DDR3, M1, MA_9	
BE8	DDR3, M1, MA_8	
BE9	DDR3, M1, MA_7	
BH6	DDR3, M1, MA_6	
BD12	DDR3, M1, MA_5	DOR3_M1, DO_63
BH7	DDR3, M1, MA_4	
BJ6	DDR3, M1, MA_3	
BC12	DDR3, M1, MA_2	
BB7	DDR3, M1, MA_0	
BF2	DDR3, M1, BS_2	
AY14	DDR3, M1, BS_1	
BH8	DDR3, M1, BS_0	
BG9	DDR3, M1, CASB	
BA14	DDR3, M1, RASB	
AY16	DDR3, M1, WEB	
AY16	DDR3, M1, CSB_1	
BD16	DDR3, M1, CSB_0	DOR3_M1, DO_48
BF16	DDR3, M1, CK_1	
AY12	DDR3, M1, CK_0	
AY12	DDR3, M1, CKE_1	
BD14	DDR3, M1, CK_0	
BF14	DDR3, M1, CKB_0	
BF10	DDR3, M1, CKE_0	
AT24	RSVD1	
AU28	RSVD2	
AV18	DDR3, M1, ODT_0	
BA16	DDR3, M1, ODT_1	DOR3_M1, DO_30
AT26	DDR3, M1, OCACVREF	
AU26	DDR3, M1, ODDVREF	
BA12	DDR3, M1, DRAMRSTB	
AV26	DDR3, VCCA_PWKR0	
BA26	DDR3, M1, RCOMFDP	
BH24	DDR3, M1, DM_23	
BD26	DDR3, M1, DM_22	
AY16	DDR3, M1, DM_6	
AY16	DDR3, M1, DM_5	
BA1	DDR3, M1, DM_4	
AP10	DDR3, M1, DM_2	
AP2	DDR3, M1, DM_1	DOR3_M1, DO_15
AP2	DDR3, M1, DM_0	
BH22	DDR3, M1, DQS_7	
BC24	DDR3, M1, DQS_7	
BC22	DDR3, M1, DQS_6	
AT20	DDR3, M1, DQS_2	
BH14	DDR3, M1, DQS_5	
BG15	DDR3, M1, DQS_4	
AY2	DDR3, M1, DQS_4	
BA3	DDR3, M1, DQS_3	
AT12	DDR3, M1, DQS_3	DOR3_M1, DO_5
AT13	DDR3, M1, DQS_2	
AV6	DDR3, M1, DQS_1	
AM2	DDR3, M1, DQS_0	
AM3	DDR3, M1, DQS_0	

\*BSW\_MCP\_EDS

2 of 13




5..8,10,12,21,24..27,31,32	+1.8VS5	
5,18,24,25,31	+1.8V	
14..27,34,35	+3V	
2,3,5,10,20,24..27,29,31..35	+3VS5	



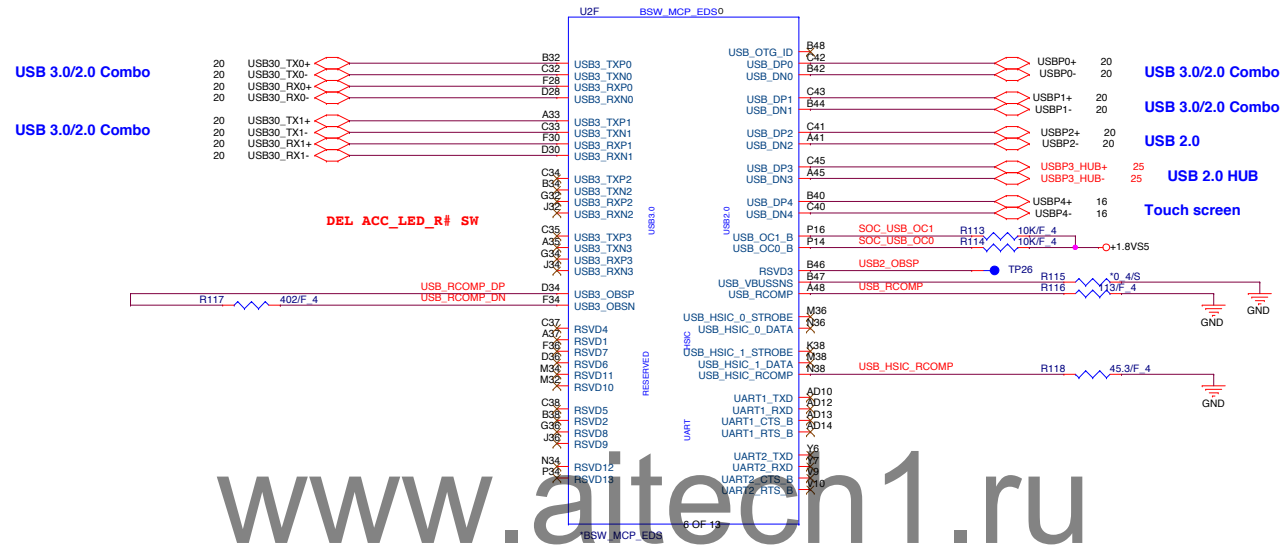
[illegible]

**For EMI**

	<h1 style="text-align: center;">PROJECT : 0P1</h1> <h2 style="text-align: center;">Quanta Computer Inc.</h2>		
	Size Custom	Document Number 05 -- Braswel 4/11(SP/PC/SA/AU)	Rev 1A
	Date: Wednesday, March 08, 2017   Sheet 5 of 35		




1/9 Board ID8 : no stuff R8033 and stuff R8034.  
it's the default setting for ODD detect function .



4,6,8,10,12,21,24,27,31,32

+1.8VSS

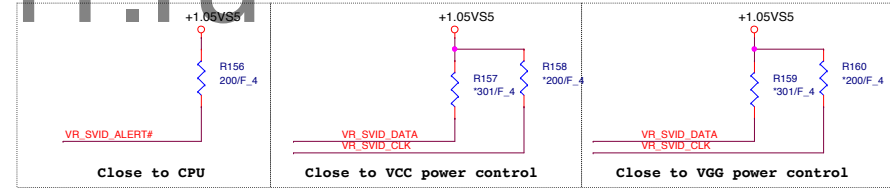
 <b>PROJECT : 0P1</b> Quanta Computer Inc.		
Size Custom	Document Number 07 -- Braswel 8/11 (USB/URAT)	Rev 1A
Date:	Wednesday, March 08, 2017	Sheet 7 of 35

The schematic diagram shows the internal structure of the RTC module and its connection to the GPIO pin. The RTC module is represented by a block labeled 'RTC' with two pins: 'RTC\_X1' and 'RTC\_X2'. The 'RTC\_X1' pin is connected to a 10M $\Omega$  resistor (R126) and a 32.768KHz/20ppm crystal (Y2). The 'RTC\_X2' pin is connected to a 2N resistor (R127) and a 32.768KHz/20ppm crystal (Y2). The crystal is connected to two capacitors: C18 (15pF/50V 4) and C20 (15pF/50V 4). The capacitors are connected to GND. A note indicates that the capacitance of C18 and C20 should be changed to 15pF. The RTC module is also connected to a 1.8VSS supply.

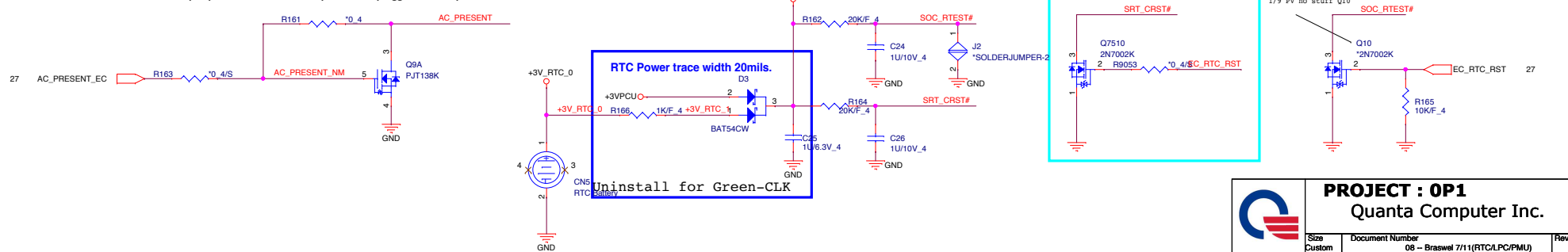
The GPIO pin is connected to the RTC module via a 10K $\Omega$  resistor (R131). The GPIO pin is also connected to a 1.8VSS supply via a 10K $\Omega$  resistor (R132). The GPIO pin is labeled 'GPIO\_J20'.


The schematic also shows the connection of the RTC module to the SOC module. The SOC module is represented by a block labeled 'SOC' with several pins: 'SOC\_REST\_BTN', 'SOC\_PLTRST#', 'PMU\_BATLOW#\_R', 'SUS\_PWDOWNACK', 'SOC\_PMC\_WAKE', 'AC\_PRESENT', 'CORE\_PWRCK', 'SUS\_PWDOWNACK', 'AC\_PRESENT', and 'SOC\_RSMRST#'. The pins are connected to various resistors and capacitors. The 'SOC\_REST\_BTN' pin is connected to a 2.2K $\Omega$  resistor (R135) and a 1.8VSS supply. The 'SOC\_PLTRST#' pin is connected to a 1K $\Omega$  resistor (R138) and a 1.8VSS supply. The 'PMU\_BATLOW#\_R' pin is connected to a 20K $\Omega$  resistor (R140). The 'SUS\_PWDOWNACK' pin is connected to a 10K $\Omega$  resistor (R142). The 'SOC\_PMC\_WAKE' pin is connected to a 10K $\Omega$  resistor (R145). The 'AC\_PRESENT' pin is connected to a 2.2K $\Omega$  resistor (R149) and a 1.8VSS supply. The 'CORE\_PWRCK' pin is connected to a 100K $\Omega$  resistor (R153) and a 1.8VSS supply. The 'SUS\_PWDOWNACK' pin is connected to a 100K $\Omega$  resistor (R153). The 'AC\_PRESENT' pin is connected to a 10K $\Omega$  resistor (R154). The 'SOC\_RSMRST#' pin is connected to a 100K $\Omega$  resistor (R155) and a 1.8VSS supply. The 'CORE\_PWRCK' pin is also connected to a 100K $\Omega$  resistor (R155) and a 1.8VSS supply. A note indicates that the capacitance of the capacitors should be changed to 100K.

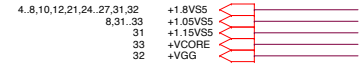
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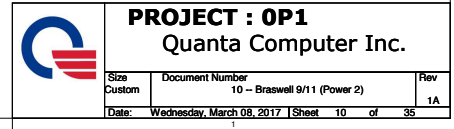


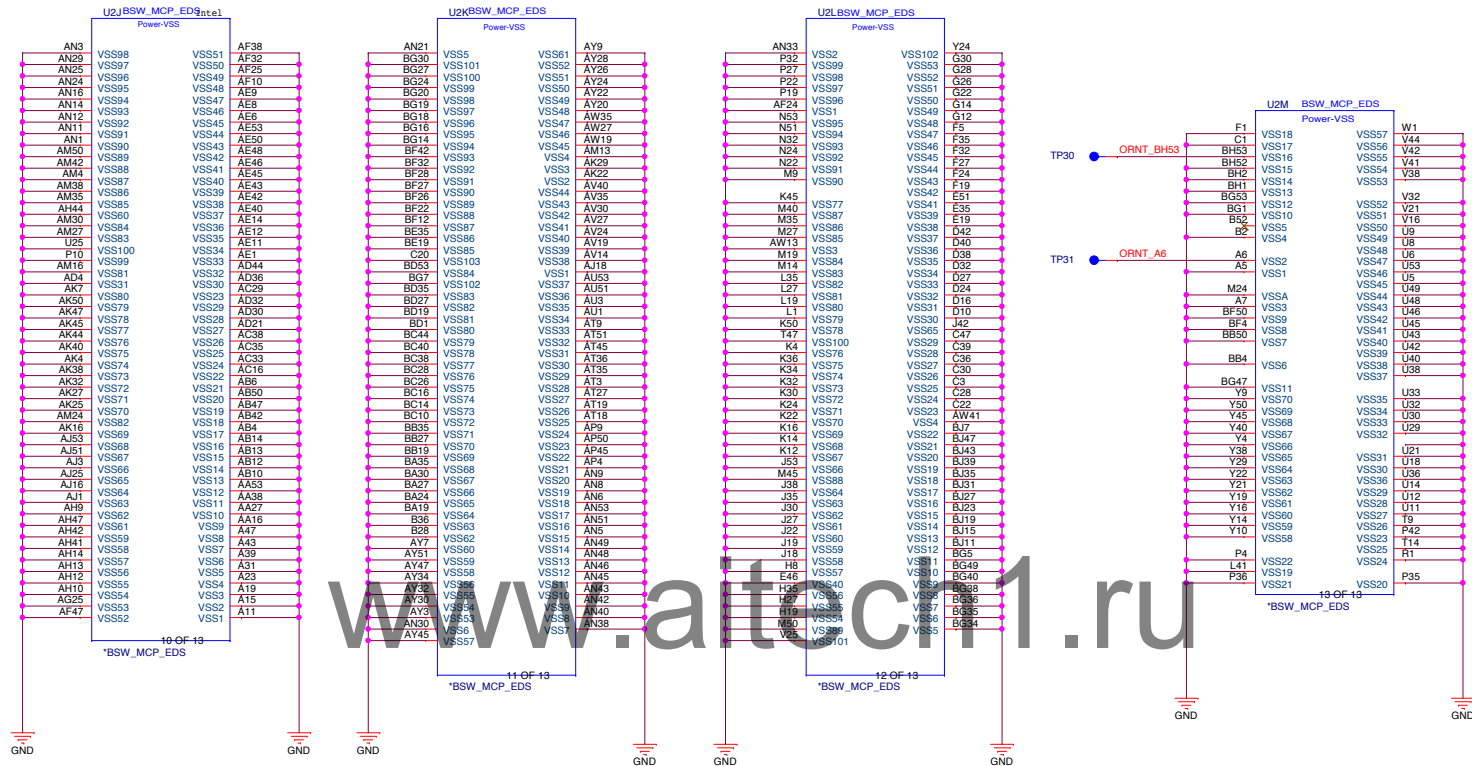
**AC Present:** This input pin indicates when the platform is plugged into AC power.

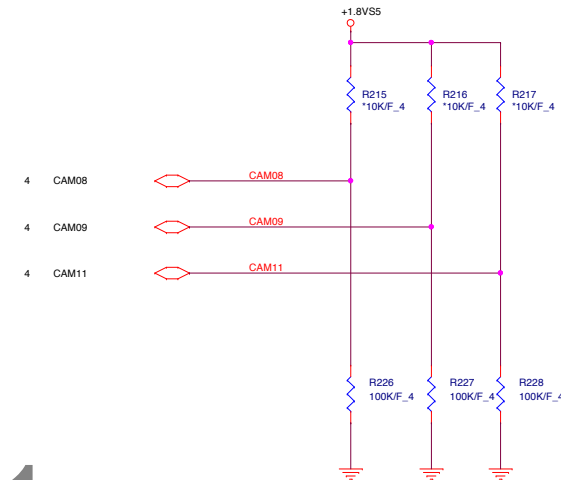
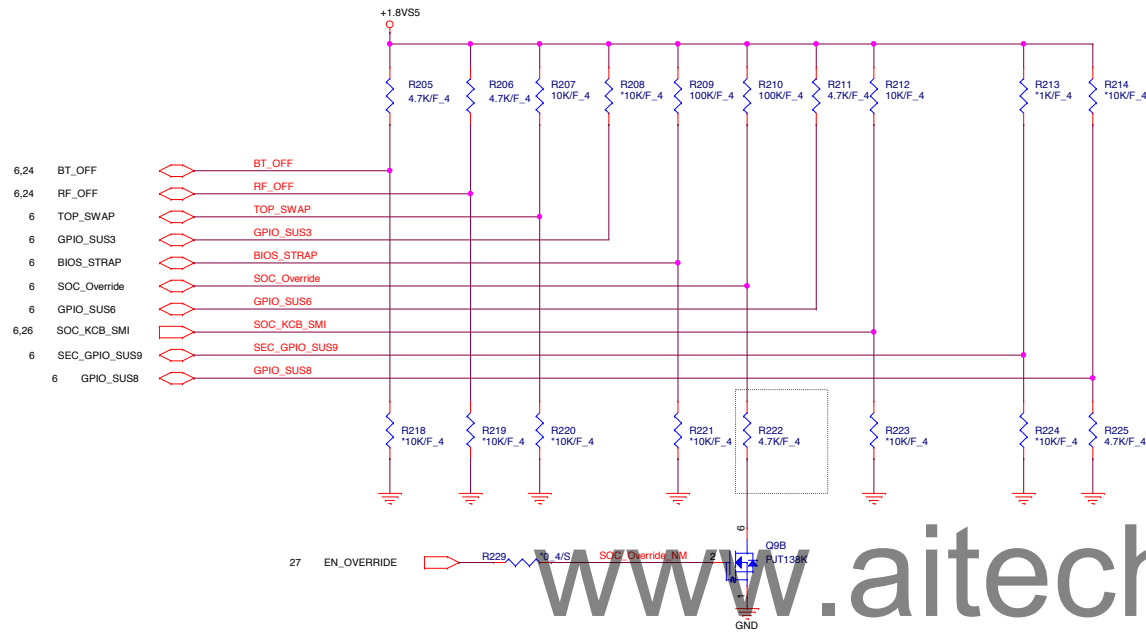


	<h1 style="text-align: center;">PROJECT : 0P1</h1> <h2 style="text-align: center;">Quanta Computer Inc.</h2>		
	Size Custom	Document Number 08 - Braswel 7/11(RTC/LPC/PMU)	Rev 1A
	Date: Wednesday, March 08, 2017	Sheet 8 of 35	









#### REQUIRED STRAPS

	GPIO_SUS0	GPIO_SUS1	TOP_SWAP	GPIO_SUS3	BIOS_STRAP	SOC_Override	GPIO_SUS6	SOC_KCB_SMI	GPIO_SUS8
<b>PULL HIGH</b>	DDI0 detected DEFAULT	DDI1 detected DEFAULT	Normal Operation DEFAULT	Reserve 10 KΩ PU DEFAULT	SPI DEFAULT	Normal Operation DEFAULT 20150209 PV change	10 KΩ PU to 1.8V DEFAULT	Reserve 10 KΩ PU DEFAULT	Supply is 1.35V
<b>PULL LOW</b>	DDI0 not detected	DDI1 not detected	Change Boot Loader address		LPC	Override			Supply is 1.25V DEFAULT

	CAM08	CAM09	CAM11
<b>PULL HIGH</b>	ICLK Xtal OSC Bypass	CCU SUS RO Bypass	RTC OSC Bypass
<b>PULL LOW</b>	ICLK Xtal OSC No Bypass DEFAULT	CCU SUS RO No Bypass DEFAULT	RTC OSC No Bypass DEFAULT

4,8,10,21,24,27,31,32

+1.8VSS



**PROJECT : 0P1**  
Quanta Computer Inc.

Size	Document Number	Rev
Custom	12 -- Braswell 11/11 (Strap)	1A
Date:	Wednesday, March 08, 2017	Sheet 12 of 35



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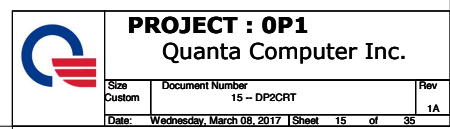
20141031: DB  
Del U15, U39, U38, U37, U40  
Del R216, R662, R159, R656, R709



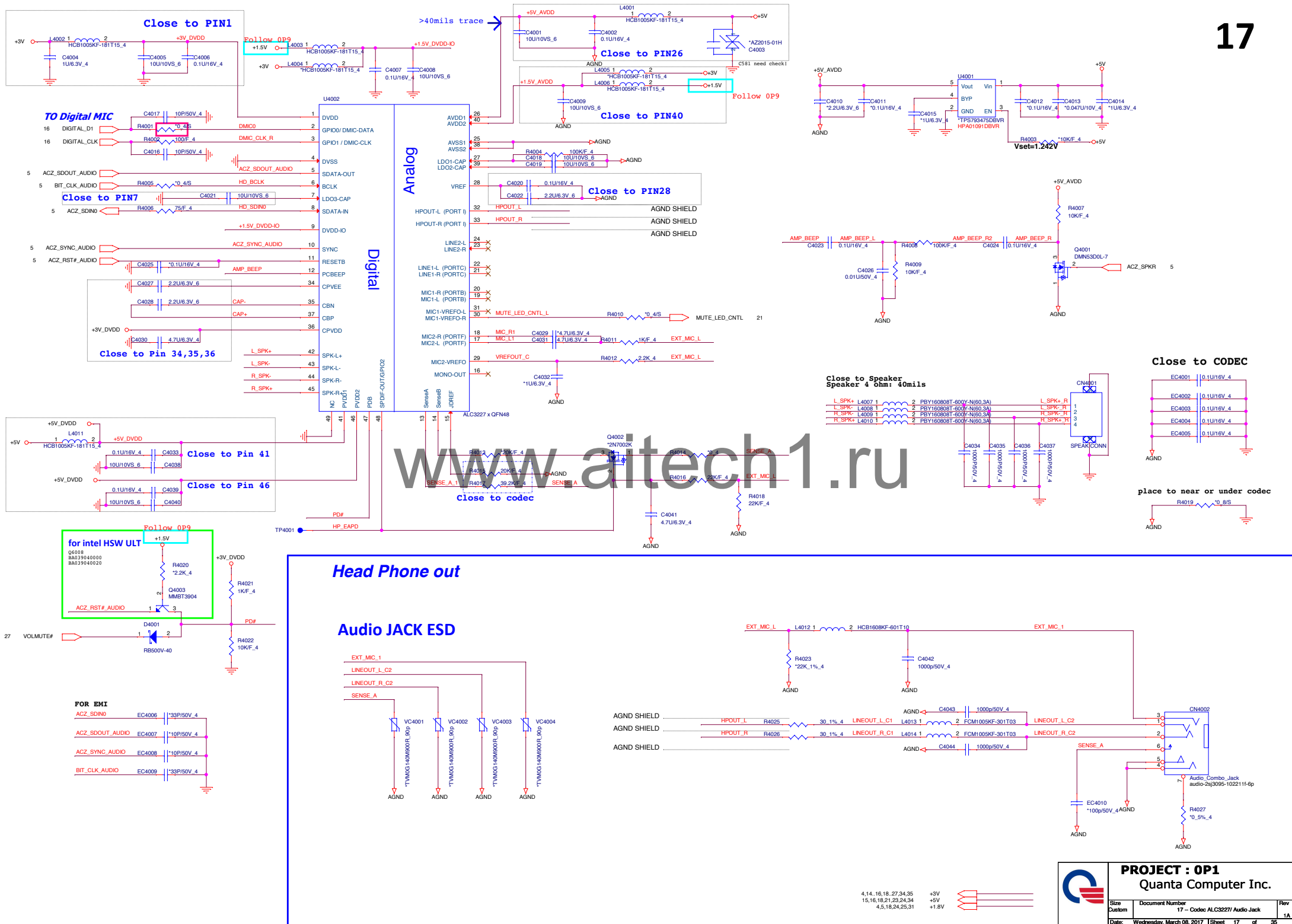
**PROJECT : 0P1**  
**Quanta Computer Inc.**

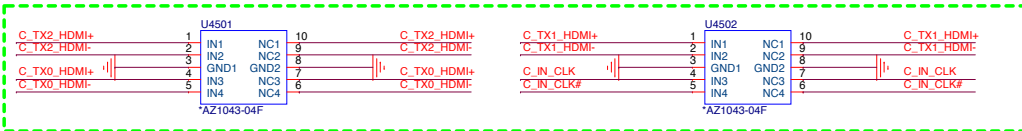
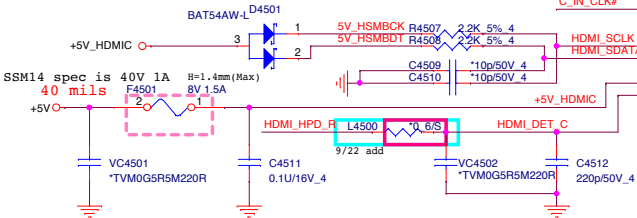
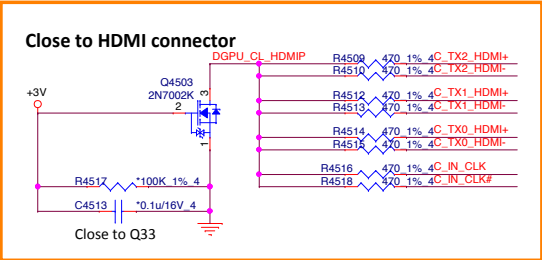
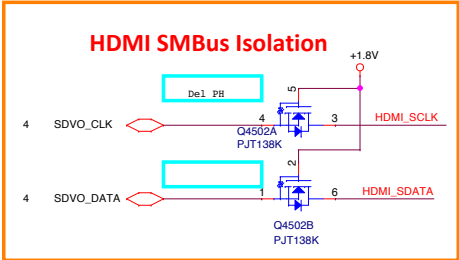
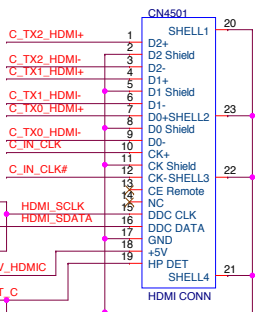
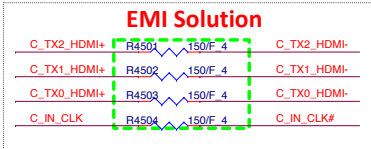
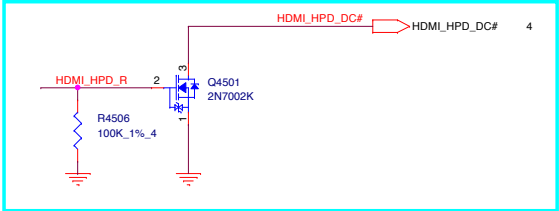
Size C	Document Number 13 - BSW XDPIAPS	Rev 1A
Date: Wednesday, March 08, 2017 Sheet 13 of 35		



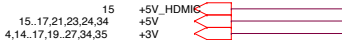







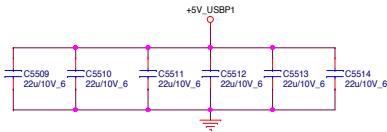
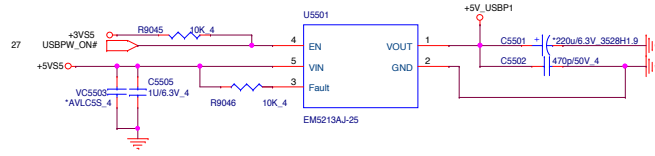


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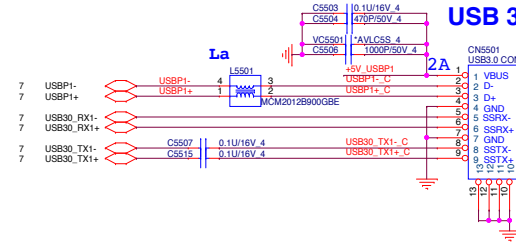
	<b>PROJECT : 0P1</b> <b>Quanta Computer Inc.</b>		
	Size Custom	Document Number HDMI	Rev 1A
Date: Wednesday, March 08, 2017		Sheet 18 of 35	





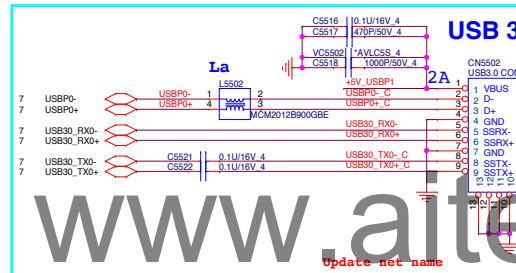
USB 2.0/3.0 Combo

USB 3.0

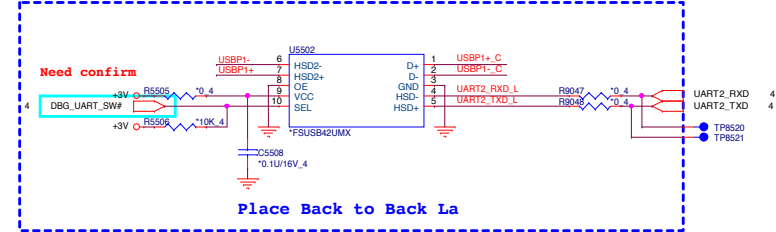


USB 2.0/3.0 Combo

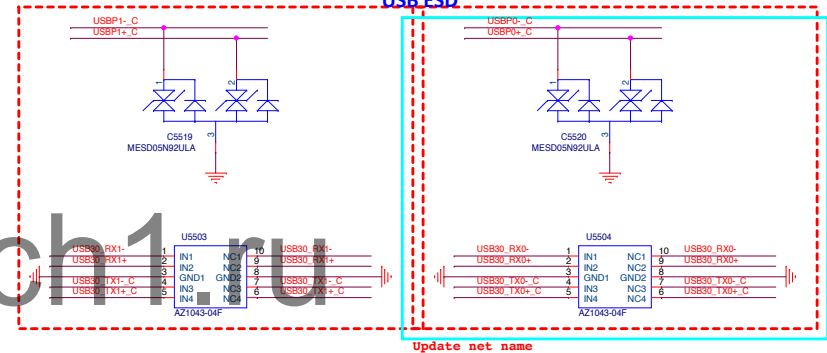
USB 3.0



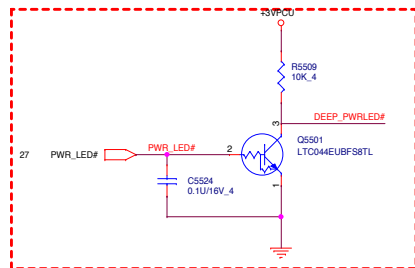
UART for Win7 WHQL DEBUG



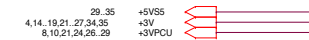
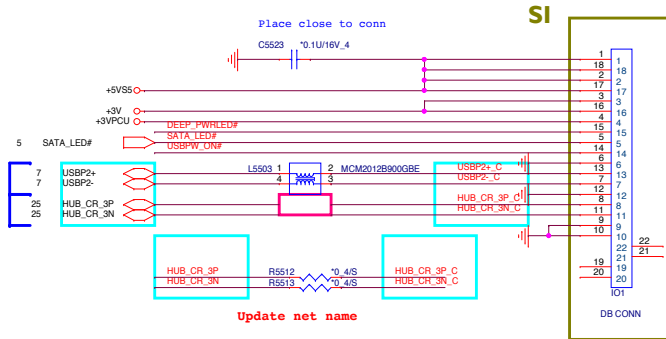
USB ESD



Daughter Board

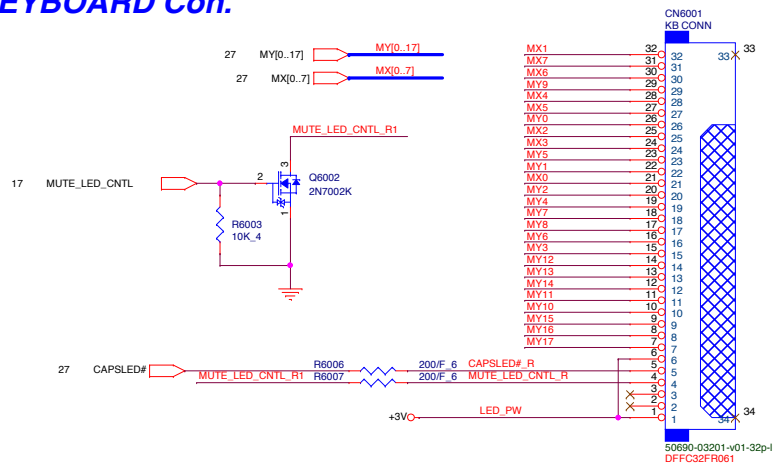


USB2 CR

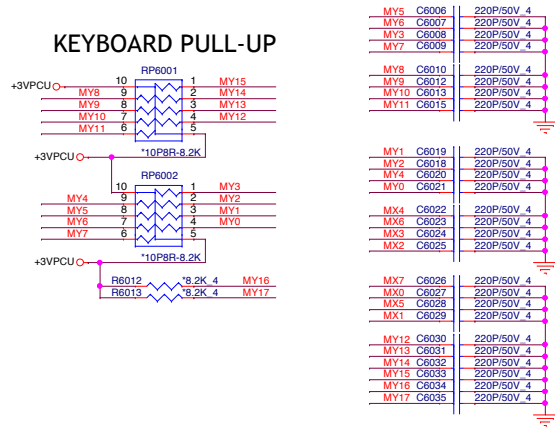




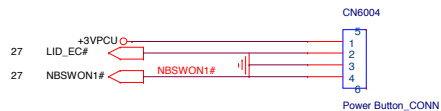
## KEYBOARD Con.



## KEYBOARD PULL-UP

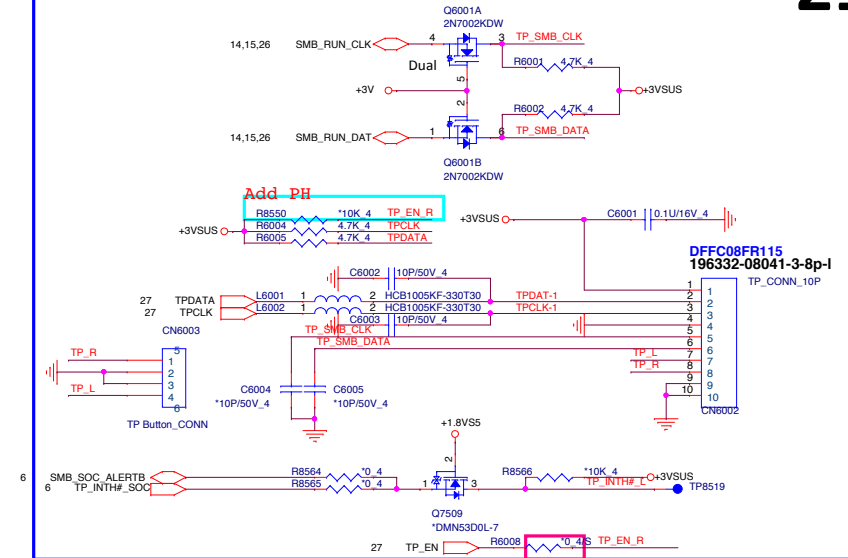


## Power Button

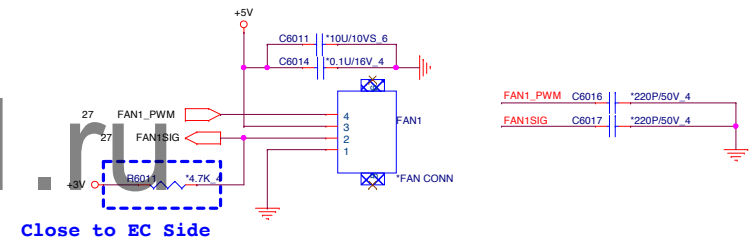







### ***Touch Pad Connector***


21



**FAN**

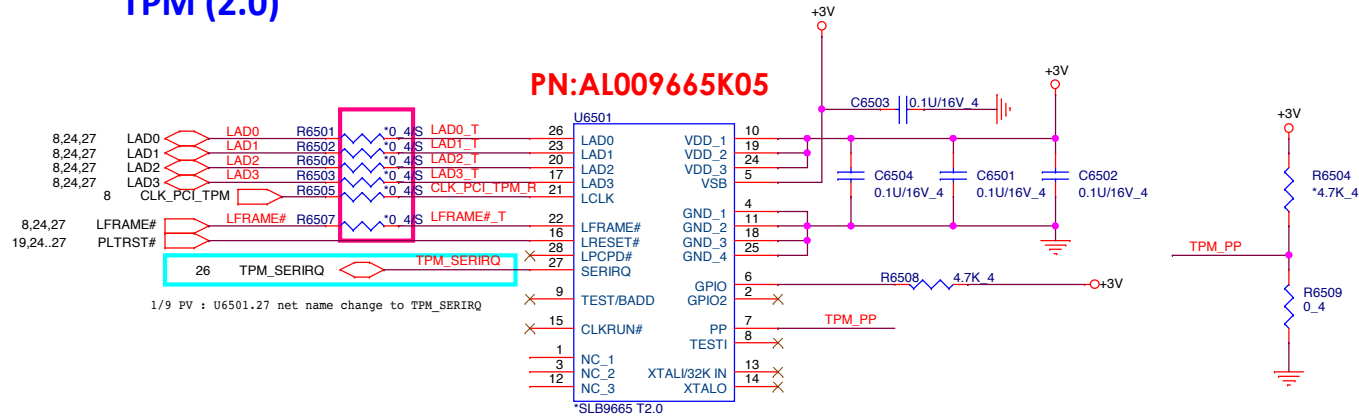


4,14..20,22..27,34,35	+3V	
8,10,20,24,26..29	+3VPCU	
15..18,23,24,34	+5V	
4,5,18,24,25,31	+1.8V	
34	+3VSUS	

	<b>PROJECT : 0P1</b> <b>Quanta Computer Inc.</b>				
	Size	Document Number			Rev
	Custom	21 -- KB/TP/FAN/POWER			1A
Date:	Wednesday, March 08, 2017	Sheet	21	of	35

# TPM (2.0)

22



USB3 to SATA VL711

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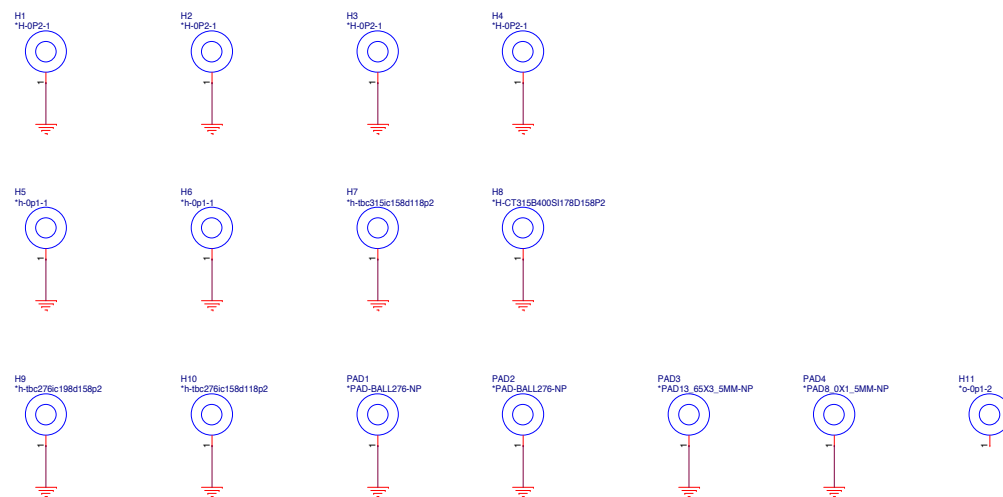
4,14..21,23..27,34,35 +3V



**PROJECT : 0P1**  
Quanta Computer Inc.

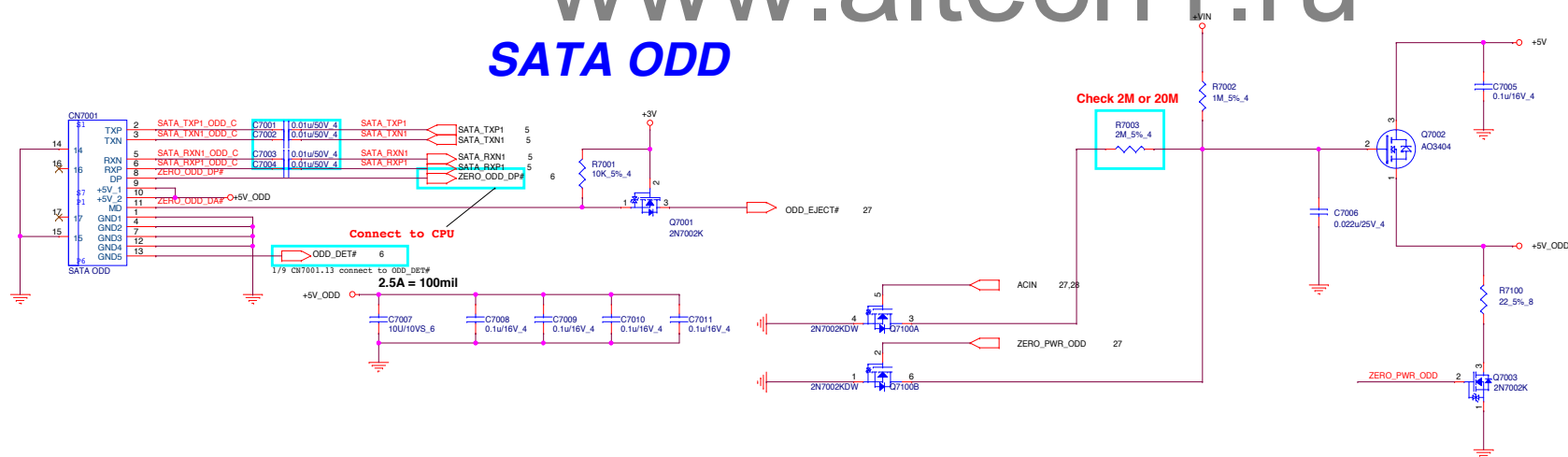
Size	Document Number	Rev
B	22 -- TPM	1A
Date:	Wednesday, March 08, 2017	Sheet 22 of 35

Hole



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SATA ODD

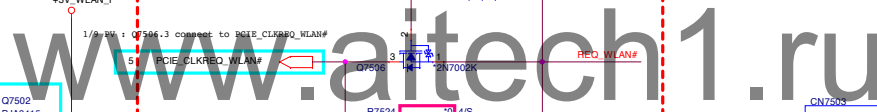


4,14, 22,24, 27,34,35 +3V  
15, 18,21,24,34 +5V  
18,28, 33,35 +VIN

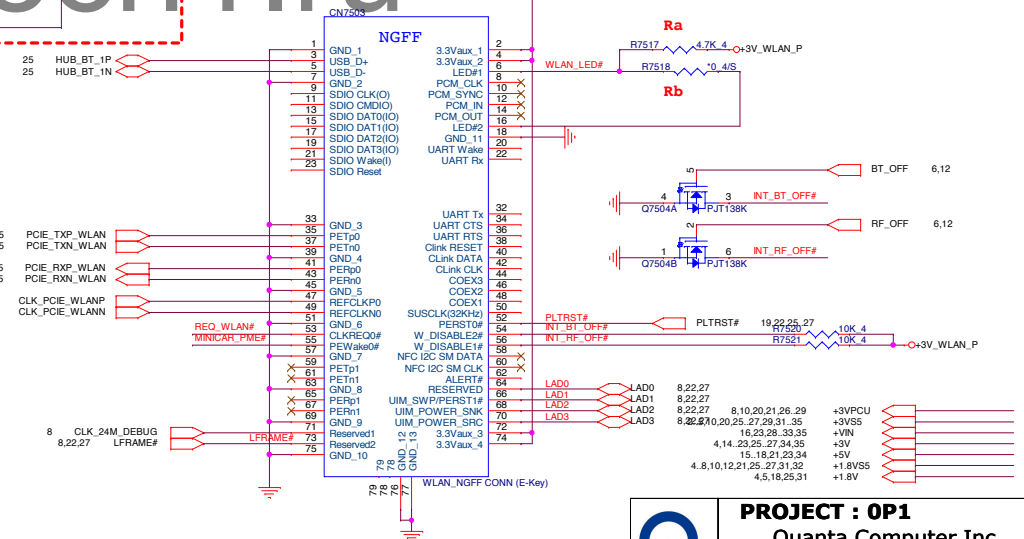



**PROJECT : 0P1**  
**Quanta Computer Inc.**

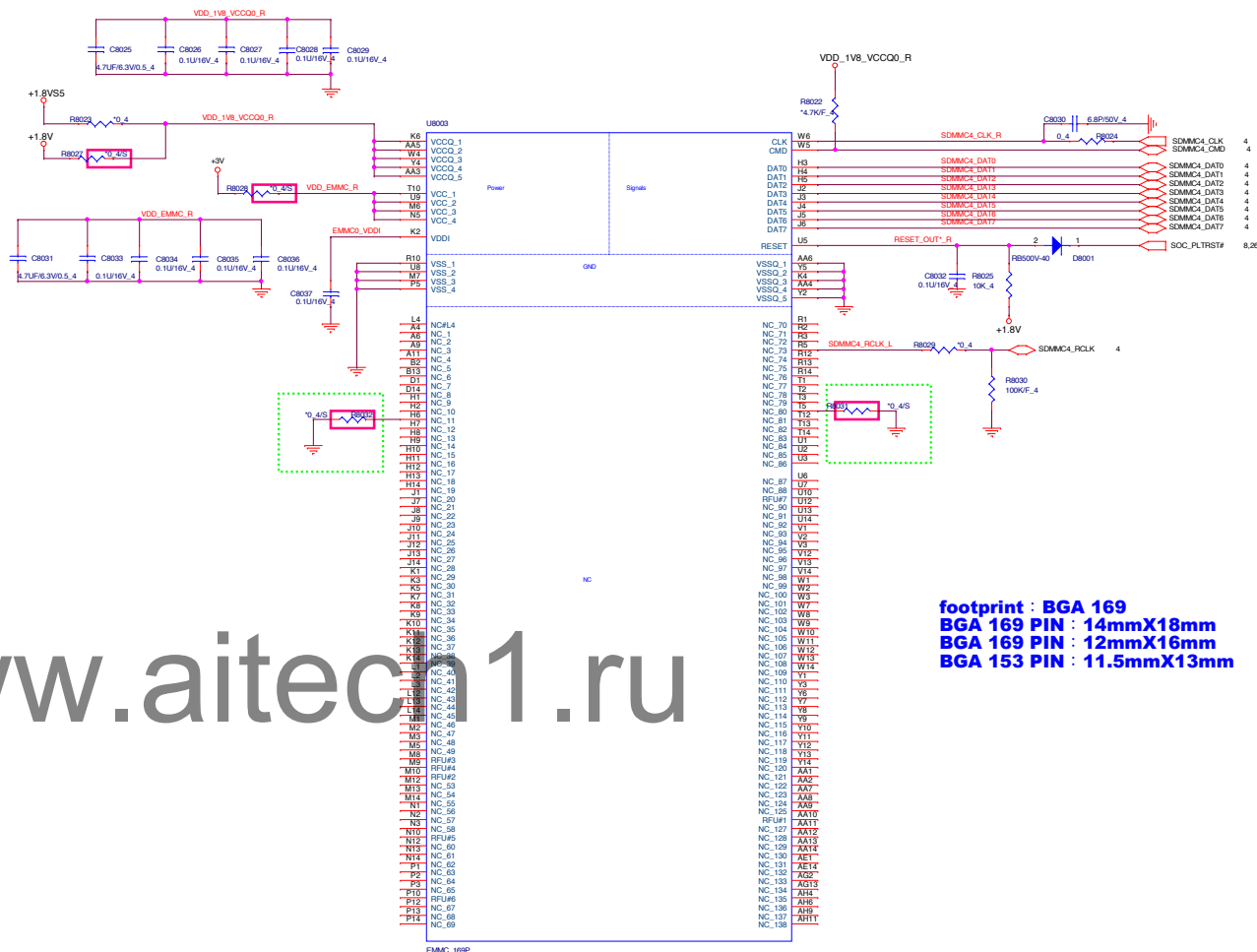
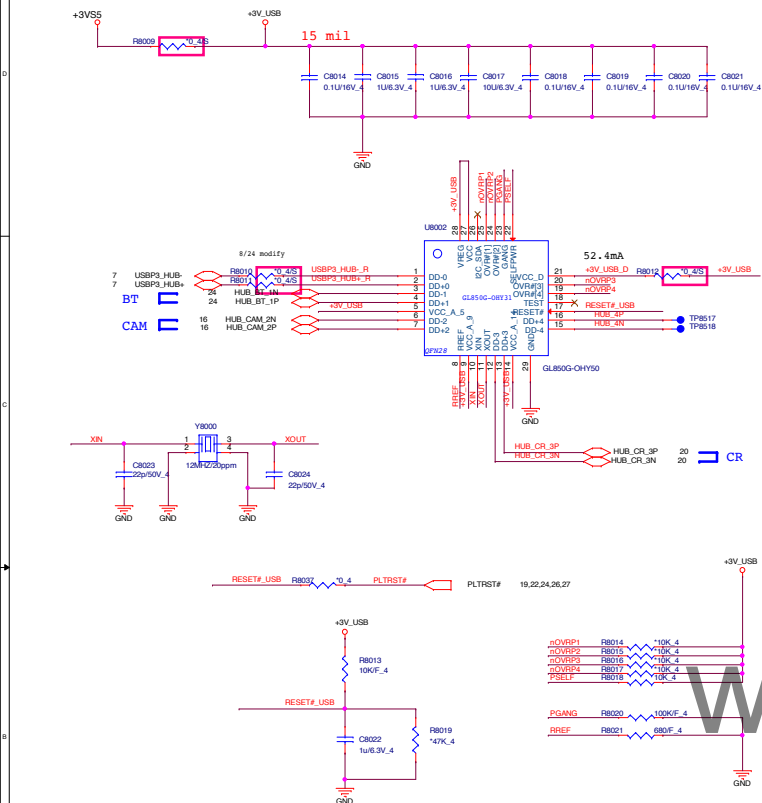
Size C	Document Number <b>23 - 2nd SSD / ODD</b>	Rev 1A
Date: Wednesday, March 08, 2017 Sheet 23 of 35		



Remove Net RF\_LINK# and need check if  
Ra and Rb can be NI



	<b>PROJECT : 0P1</b> <b>Quanta Computer Inc.</b>		
	Size Custom	Document Number 24 – HDD/WLAN(NGFF)	Rev 1A
Date:	Wednesday, March 08, 2017	Sheet 24 of 35	



footprint : BGA 169  
BGA 169 PIN : 14mmX18mm  
BGA 169 PIN : 12mmX16mm  
BGA 153 PIN : 11.5mmX13mm

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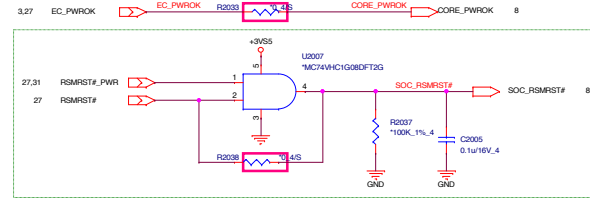
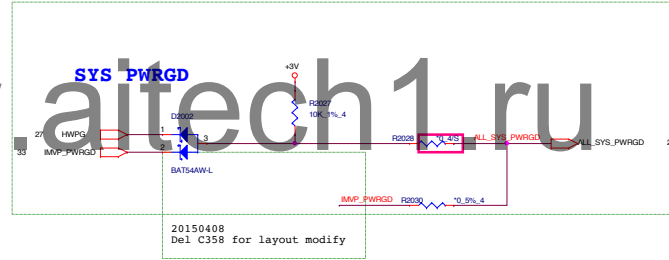
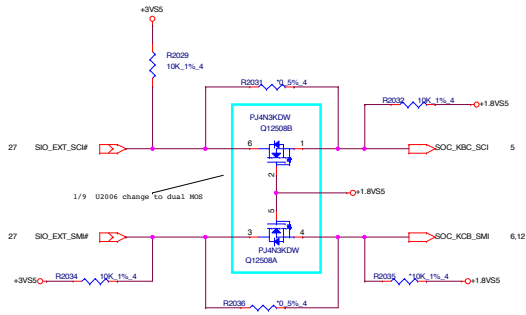
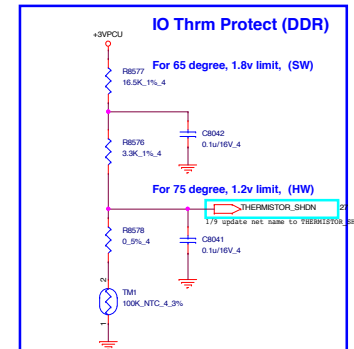
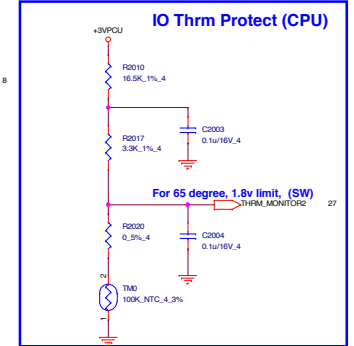
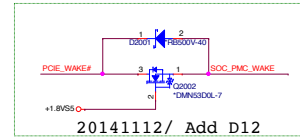
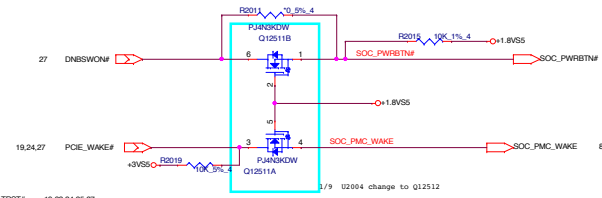
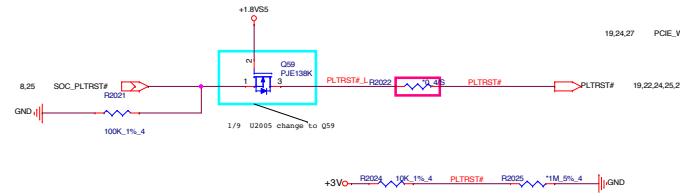
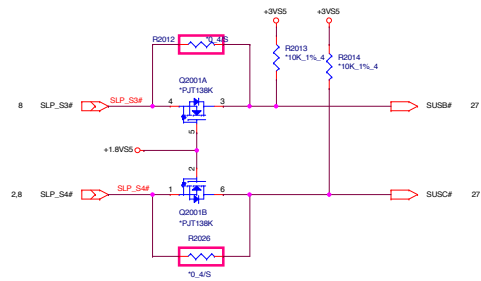
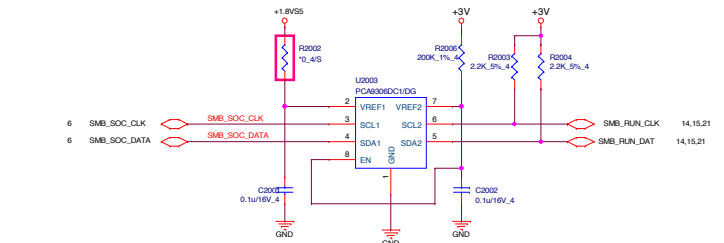
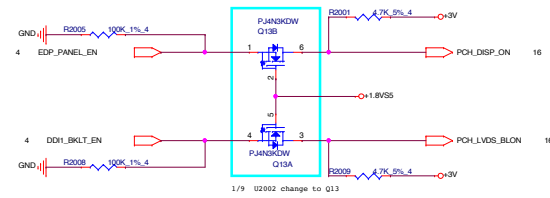
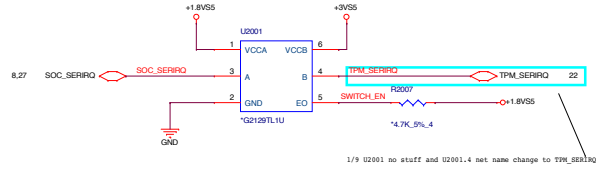
27741 - eMMC 32GB MO-276 MMCv5.0				
TOPBSQ	GBCON	Description	SIZE	Vender
AKE31Z0TW01	AKE31Z0TW00	IC FLASH(153P) H26M84208EMR(FBGA)TOP BSQ	32G	Hynix
AKE3S20T501	AKE3S20T500	IC FLASH(153P) KLM8G2JENB-B041 TOP BSQ	32G	Samsung
AKE3SF-T107	AKE3SF-T106	IC FLASH(153P) SDINAD4-32G-H TOP BSQ	32G	SanDisk
AKESS20T001	AKESS20T000	IC FLASH (153P) THGBMHG8C2LBAIL TOP BSQ	32G	Toshiba
27742 - eMMC 64GB MO-276 MMCv5.0				
AKE31Z0TW03	AKE31Z0TW02	IC FLASH(153P)H26M78208CMR(FBGA)TOP BSQ	64G	Hynix
AKE3U2FT501	AKE3U2FT500	IC FLASH(153P) KLMCG4JENB-B041 TOP BSQ	64G	Samsung
AKE31ZPT014	AKE31ZPT013	IC FLASH(153P)THGBMHG8C4BAIR TOP BSQ	64G	Toshiba

4,14, 24,26,27,34,35 +3V  
2,5,10,20,34,36,27,30,31,35 +3V55  
4,5,10,12,21,24,26,27,31,32 +1.8V55  
4,5,18,24,31 +1.8V

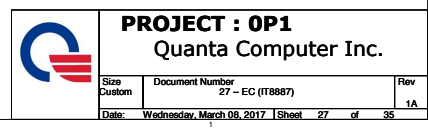
**PROJECT : 0P1**  
Quanta Computer Inc.

Size	Document Number	Rev
Custom	25 - USB HUB / eMMC	1A
Date	Wednesday, March 08, 2017	Sheet 25 of 35

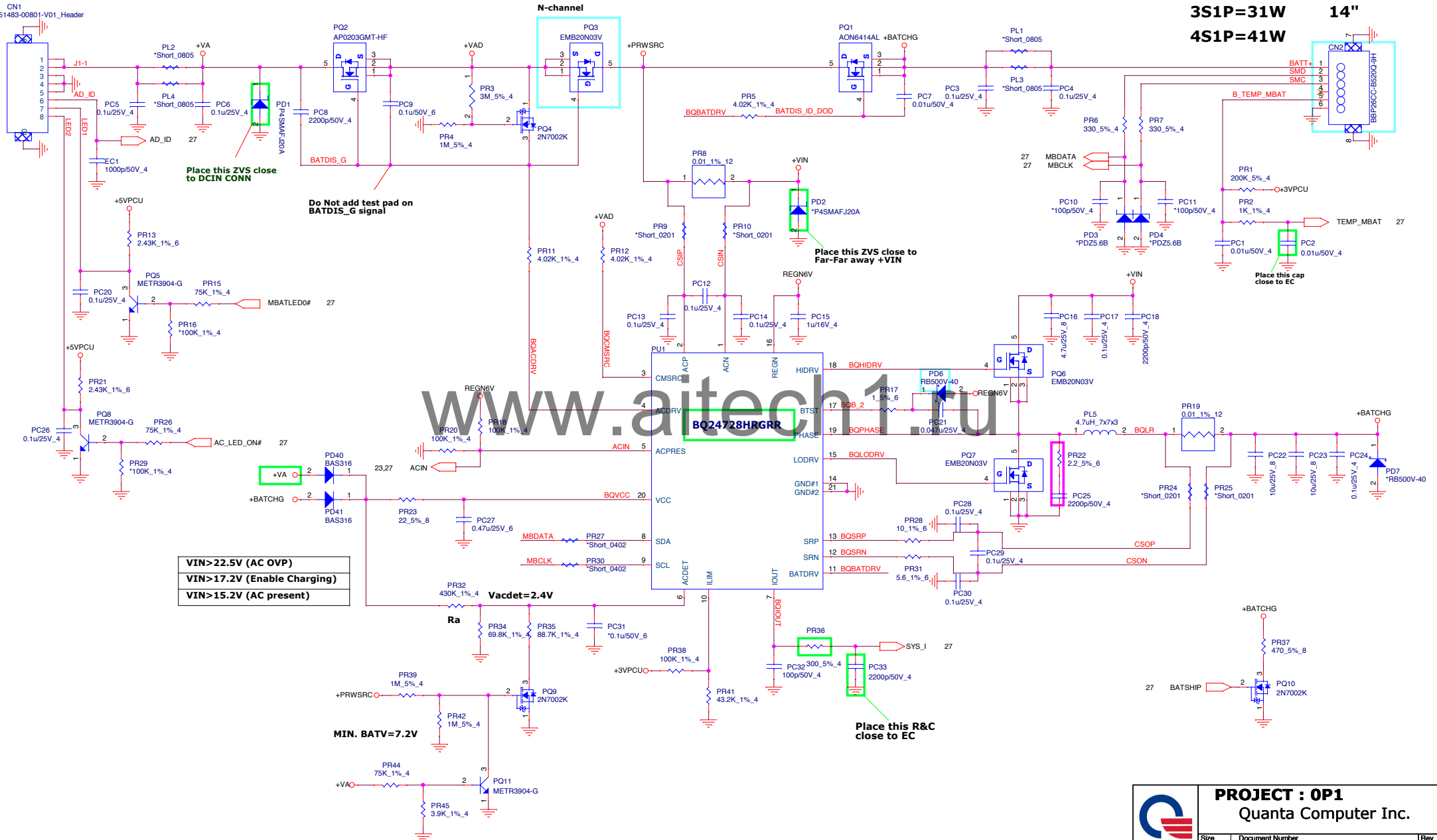
BOM : TPM SKU stuff U2001,R2007



8,10,20,21,24,27,29 +3VPCU  
2,5,10,20,24,25,27,29,31,35 +3V  
4,8,10,12,21,24,25,27,31,32 +1.8V5S  
4,5,10,24,25,31 +1.8V



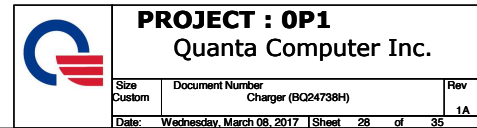
CN1  
51483-00801-V01\_Header



VIN>22.5V (AC OVP)
VIN>17.2V (Enable Charging)
VIN>15.2V (AC present)

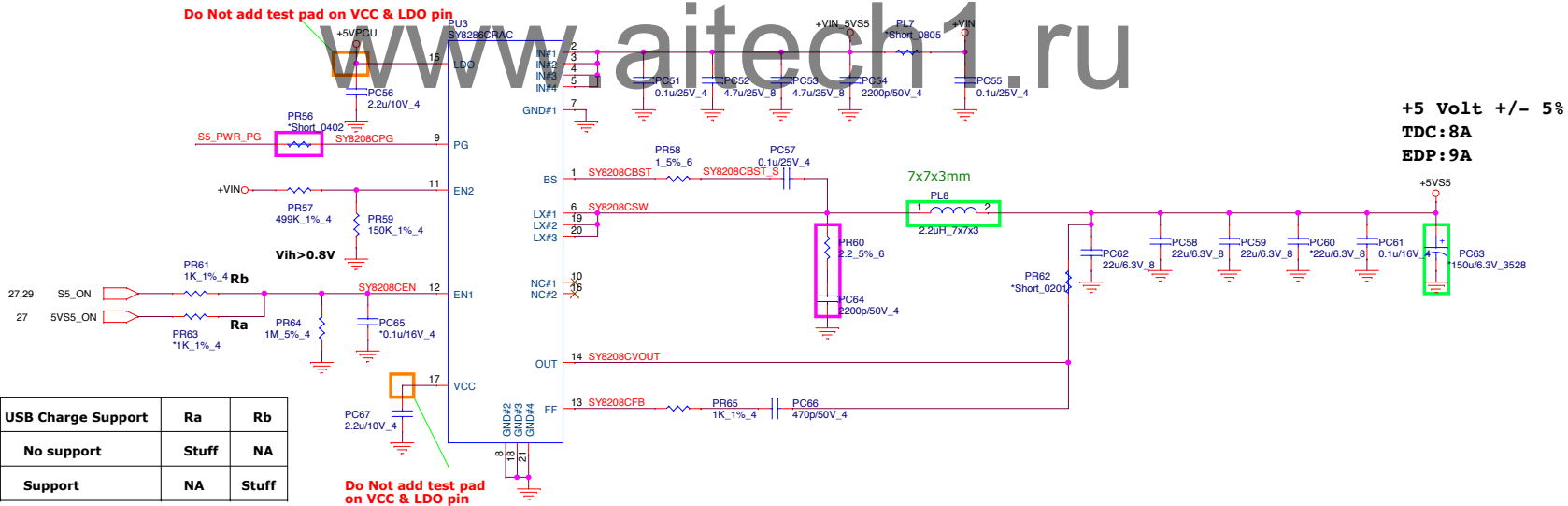
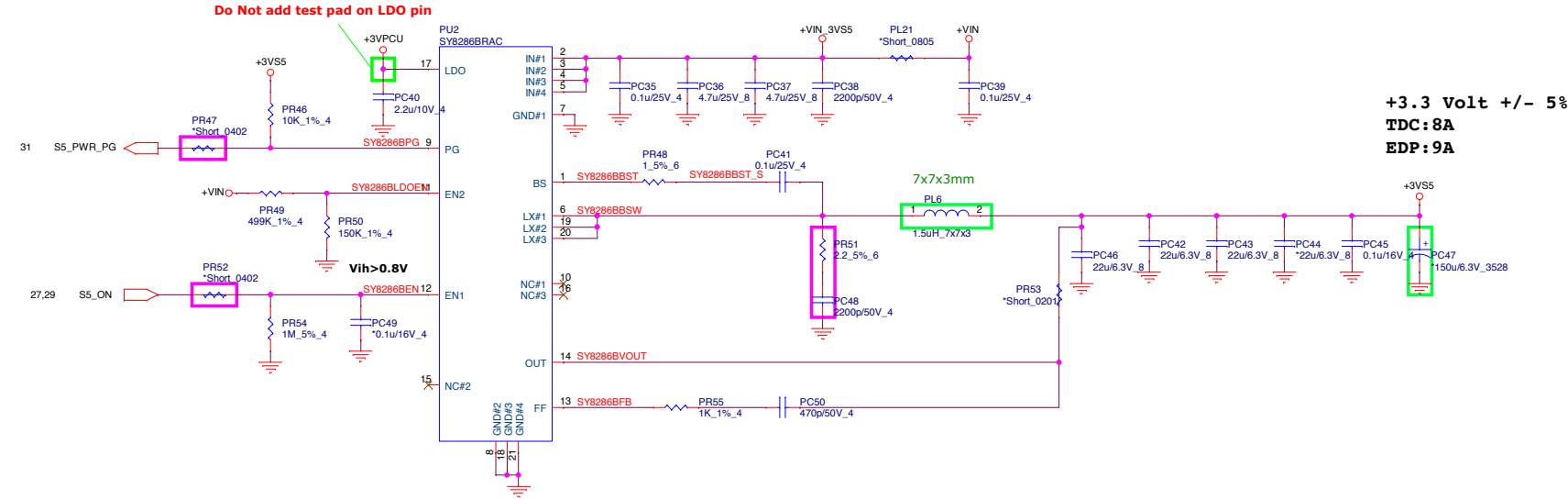
**MIN. BATV=7.2V**

**Place this R&C  
close to EC**



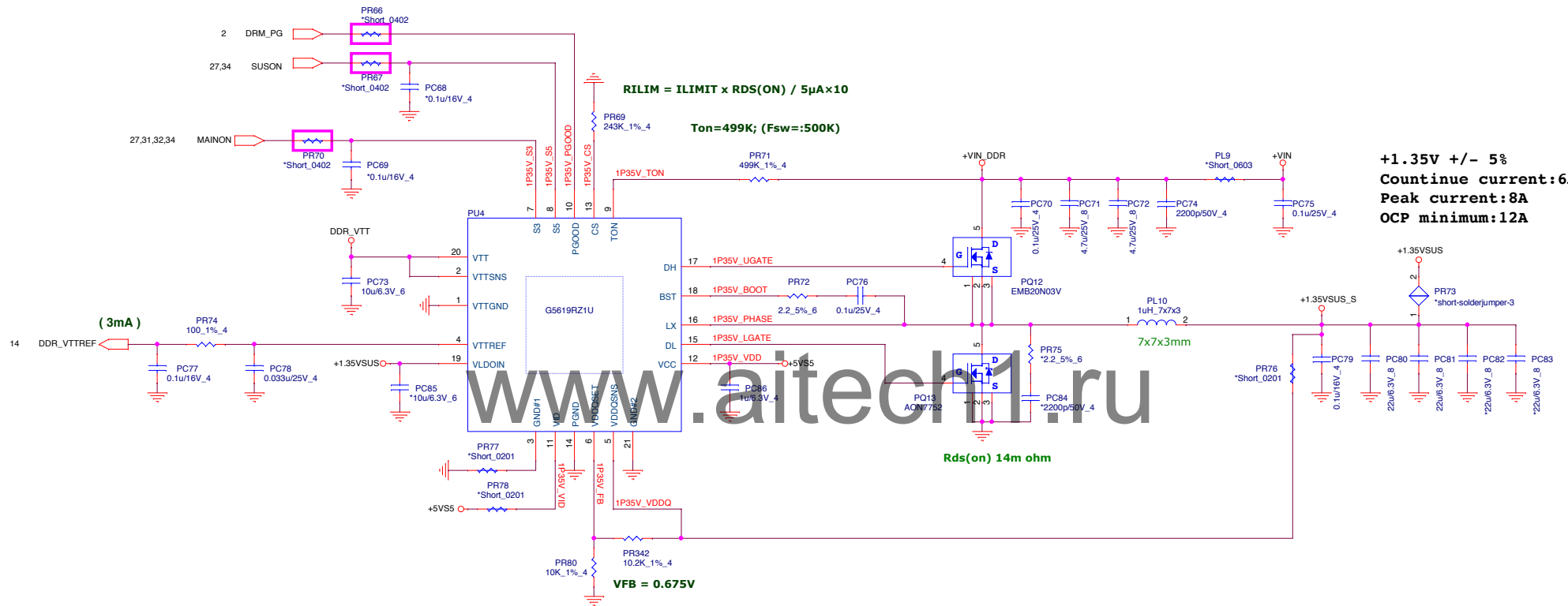


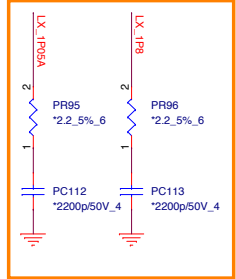
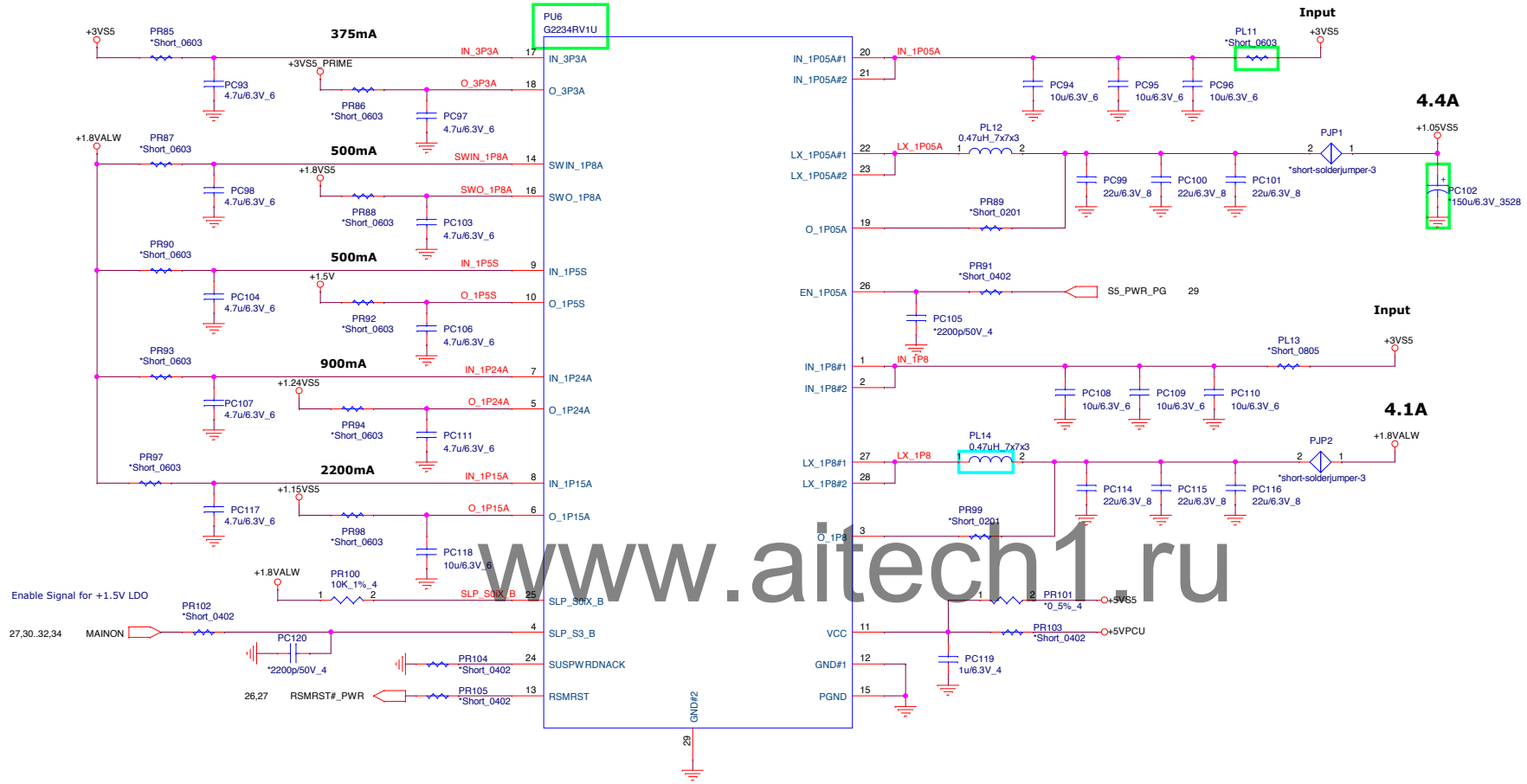
+VIN	16,23,28,30,33,35
+3VS5	2,5,10,20,24,27,31,35
+5VS5	20,30,35
+3VPCU	8,10,20,21,24,26,28
+5VPCU	28,31,34



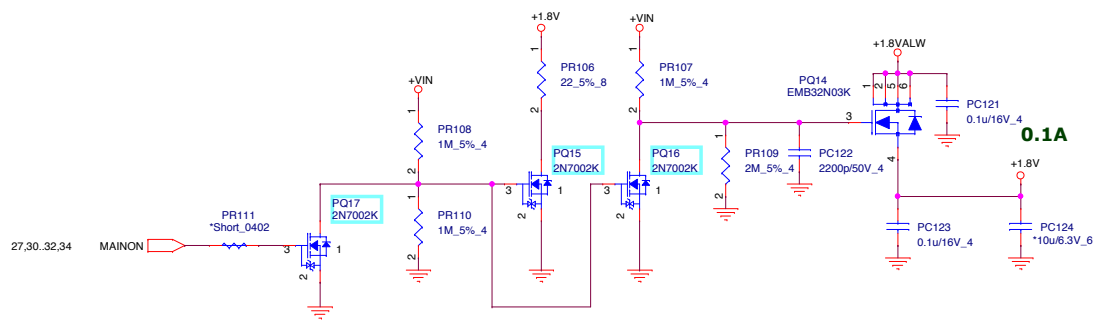
USB Charge Support	Ra	Rb
No support	Stuff	NA
Support	NA	Stuff

+VIN 16,23,28,29,31..33,35  
+5VS5 20,29,31..35  
+1.35VSUS 2,3,10,14,35  
DDR\_VTT 14





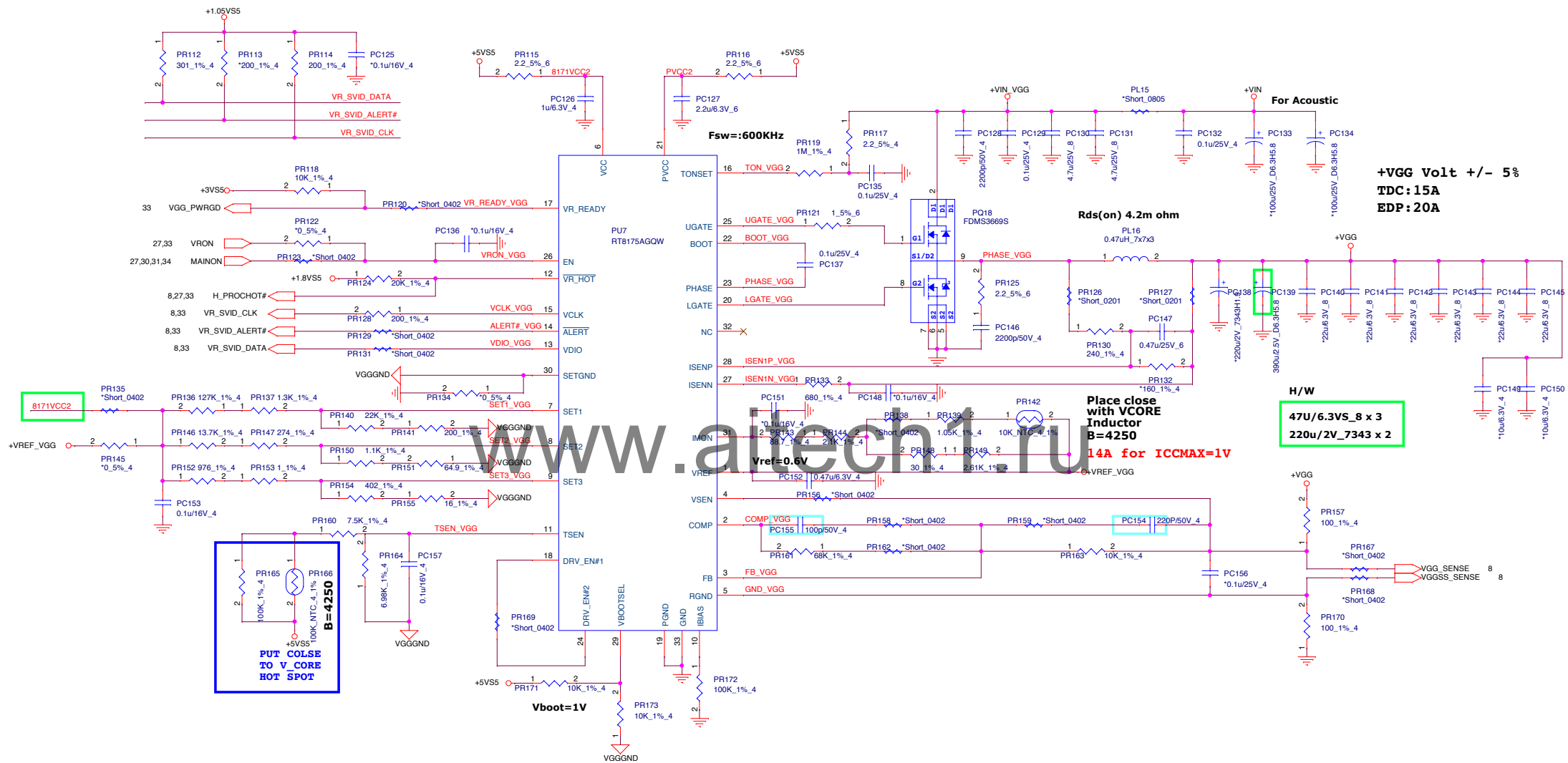
Snubber



+3VS5	2,5,10,20,24,27,29,32,35
+1.8VALW	4,8,10,12,21,24,27,32
+3VS5_PRIME	10,27
+1.5V	10,17
+1.24VS5	10
+1.15VS5	9,31
+5VPCU	28,29,31,34
+1.05VS5	8,9,32,33
+1.15VS5	9,31
+5VPCU	28,29,31,34
+1.8V	4,5,18,24,25

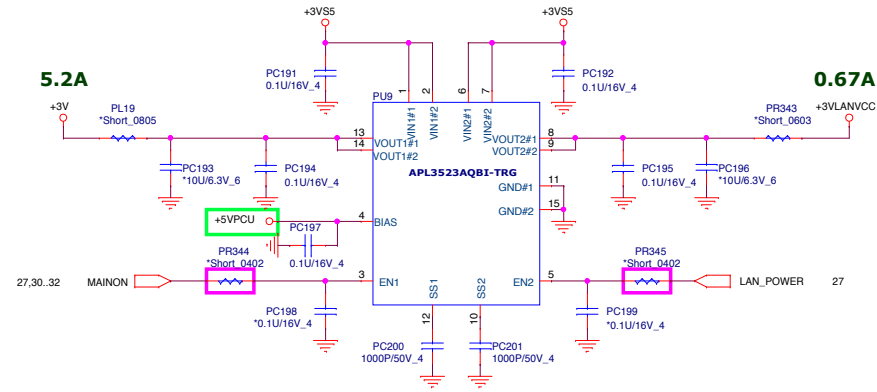
**PROJECT : OP1**  
Quanta Computer Inc.

Size	Document Number	Rev
Custom	1.05VS5/1.8VS5/1.24VS5	1A
Date:	Wednesday, March 08, 2017	Sheet 31 of 35

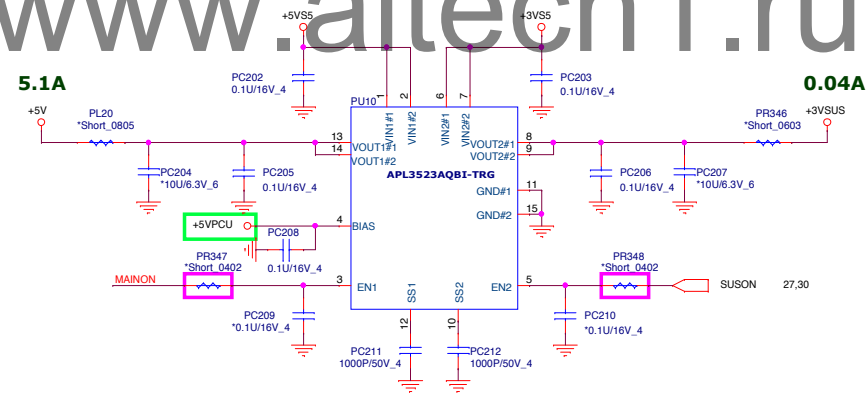




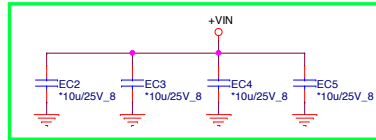
+3V	4,14,27,35
+5V	15,18,21,23,24
+VIN	16,23,28,33,35
+3VS5	2,5,10,20,24,27,29,31,33,35
+5VS5	20,29,33,35
+3VSUS	21
+5VPCU	28,29,31
+3VLAVCC	19



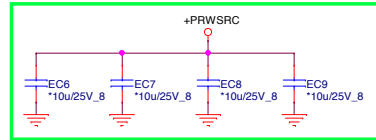
www.aitech1.ru



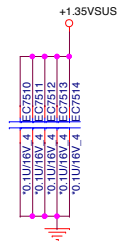
EMI request for ISN



EMI request for ISN



TOP side



BOT side



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